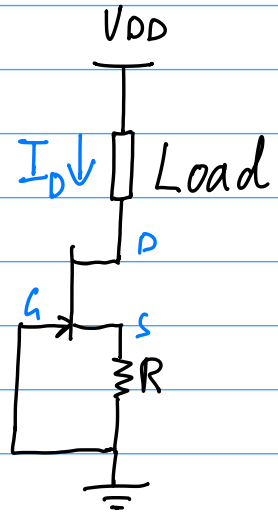
AoE 3.1

Design a 1 mA current sink using the 2N5484 JFET.

Use the circuit layout shown in Fig 3.23.



$V_{GS} = -I_D R$

We want $I_D = 1$ mA.

From Fig. 3.21A, this means $V_{GS} \approx -0.6$ V.

$\therefore \; -0.6 = -0.001 R$

$R = 600\ \Omega$.

However: JFET manufacturing variability would be a problem here. I_{DSS} ranges from 1 mA to 5 mA. This would create a lot of variation in I_D (see Fig 3.25).